SGS-THOMSON MICROELECTRONICS

**APPLICATION NOTE**

# VIPer100 THE MOST ADVANCED MONLITHIC SOLUTION FOR OFF-LINE PRIMARY CONVERTERS

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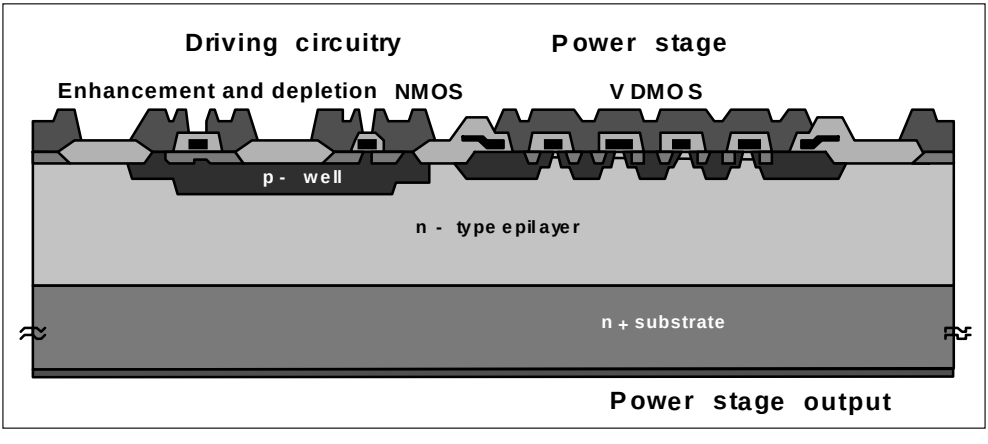
## INTRODUCTION

Following the ever increasing consumer market needs for Advanced - albeit cost effective - solutions for Off Line Switch Mode Power Supplies, SGS-THOMSON Microelectronics has developed the VIPerXX0 family of monolithic devices for SMPS applications. These devices were developed using the well consolidated VIPower® M0 technology.

VIPer100/100A and VIPer50/50A combines on the same silicon chip a state-of-the-art PWM circuit with current mode control and a dedicated compensation path together with an optimized high voltage avalanche rugged Vertical Power MOSFET. Housed in the 5 lead TO-220 as well as in the PowerSO-10 surface mounting package, they both offer maximum flexibility to designers allowing a primary or secondary regulation loop despite using around 50% less components when compared with a discrete implementation.

**Figure 1.** VIPower® M0 technology Cross Section




The VIPower® M0 technology uses enhancement and depletion N-MOS signal transistors for the logic section built into a p-well buried layer, and a Vertical DMOS power transistor as the output stage. The voltage capability for this technology ranges from 30V to 1,200V, while the vertical Power MOSFET output stage - the same as for the discrete counterpart - allows high power level handling.

Start up of the circuit is insured by an internal high voltage current source which is switched off during normal operation. Adjustable switching frequency up to 200KHz is achieved by an external R-C network. Synchronisation to an external clock generator is also possible. Built-in overtemperature protection offers excellent safety and silicon self protection in the case of abnormal operating conditions.

Burst mode operation is an additional feature of this device, offering the possibility to operate in stand-by mode without extra components and allowing the VIPerXX0 to meet the new Germany's "Blue Angel" Eco Norm with less than 1W total power dissipation for the system when working in that condition.

| TYPE | $BV_{DSS}$ | $I_{Dmin}$ | $R_{DS(on)}$ @ $T_J = 25^0C$ |
|---|---|---|---|
| VIPer100/SP | 600V | 3A | 2.5Ω @ $I_D = 2A$ |
| VIPer 100A/ASP | 670V | 3A | 3.3Ω @ $I_D = 2A$ |
| VIPer50/SP | 600V | 1.5A | 5 Ω@ $I_D = 1A$ |
| VIPer 50A/ASP | 670V | 1.5A | 6.6Ω @ $I_D = 1A$ |

The VIPer100 can be efficiently used for implementing a current mode flyback configuration in the discontinuous inductor current mode, with a power capability of 100W on a European voltage range (180 to 270VAC) and 50W for a universal input voltage range (85 to 270VAC).

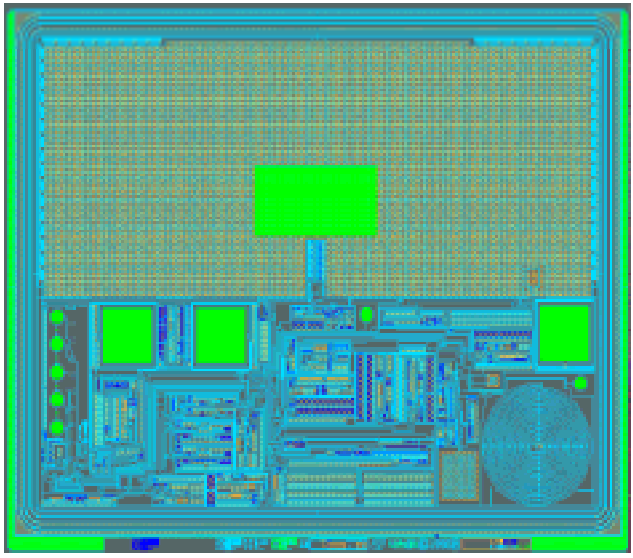
Set Top Box Satellite Receivers, Decoders, Video Recorders, Digital Video Disk, Laptops, Monitors, Camcorders, Television sets, Battery chargers, and Open frame power supply represent only a small selection of products that can be easily equipped with a VIPerXX0 benefitting from all the advantages of the best integrated solution available on the market.

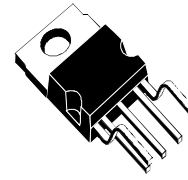
There is a greatly increased overall reliability of the system due to an approximately 50% reduction in the components used with respect to a similar discrete implementation and complete protections built into the silicon.

Additional advantages of VIPerXX0 family devices, when compared to existing monolithic solutions, include:

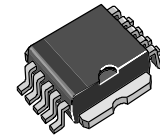
a) The useful duty cycle range extends from 0 to about 90% for VIPerXX0 versus the 3% to 70% available on the market. The main benefit for users is the possibility to operate in stand-by mode with nearly zero power output.

**Figure 2.** VIPer100™ - chip layout and suitable packages





**PW-HV**



**PowerSO-10**

b) Larger regulation loop bandwidth. VIPerXX0 provides a specific path for compensation components (COMP pin), offering a maximum of freedom for the users to adjust the regulation bandwidth with good repetitivity.

c) Excellent good line regulation because of the current mode control topology.

d) Better regulation point voltage because of the higher value of this voltage when compared with monolithic solutions available on the market. This allows greater precision of the output voltage especially in the case of a primary regulation. A constant $R_{DS(ON)}$ value versus drain current is also assured.

**VIPer100 Family Highlights:**

* ADJUSTABLE SWITCHING FREQUENCY UP TO 200 KHZ
* CURRENT MODE CONTROL
* SOFT START AND SHUT DOWN CONTROL
* AUTOMATIC BURST MODE OPERATION IN STAND-BY CONDITION ABLE TO MEET "BLUE ANGEL" NORM (<1W TOTAL POWER CONSUMPTION)
* INTERNALLY TRIMMED ZENER REFERENCE
* UNDERVOLTAGE LOCK-OUT WITH HYSTERESIS
* INTEGRATED START UP SUPPLY
* AVALANCHE RUGGED
* OVERTEMPERATURE PROTECTION
* LOW STAND-BY CURRENT
* ADJUSTABLE CURRENT LIMITATION

**Typical Application Circuits:**

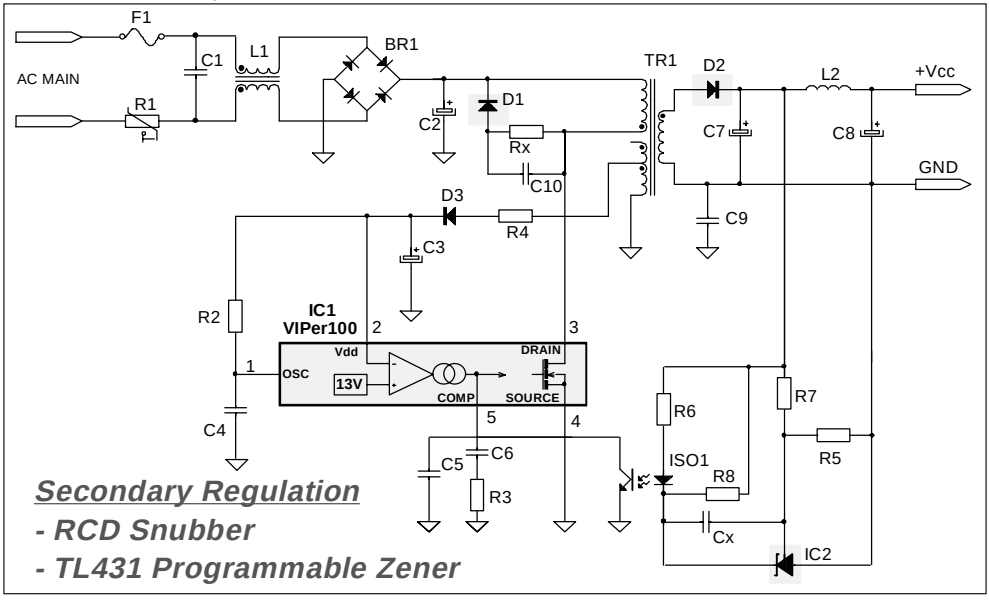
Two typical application examples for secondary and primary regulation are given for figures 3 and 4. Both circuits are current mode Flyback Converters operating in the discontinuous inductor current mode.

For both circuits the switching frequency was fixed to 100KHz.

Main advantages of the Flyback Converters operating in the discontinuous inductor current mode are:

* *All outputs will track each other within +/- 5-10% without post-regulation. Dynamic cross-regulation is also very good;*
* *The flyback transformer used in the discontinuous mode can be much smaller because the stored inductive energy is lower with respect to the energy required in comparable continuous mode circuits;*
* *Load current in the Power MOSFET output stage is zero during turn-on avoiding turn-on losses or turn-on snubber circuits. Conducted EMI is also reduced;*
* *Regulation loop is easy to compensate because of the single pole (resulting in a single capacitor filter);*
* *Transient response is excellent.*

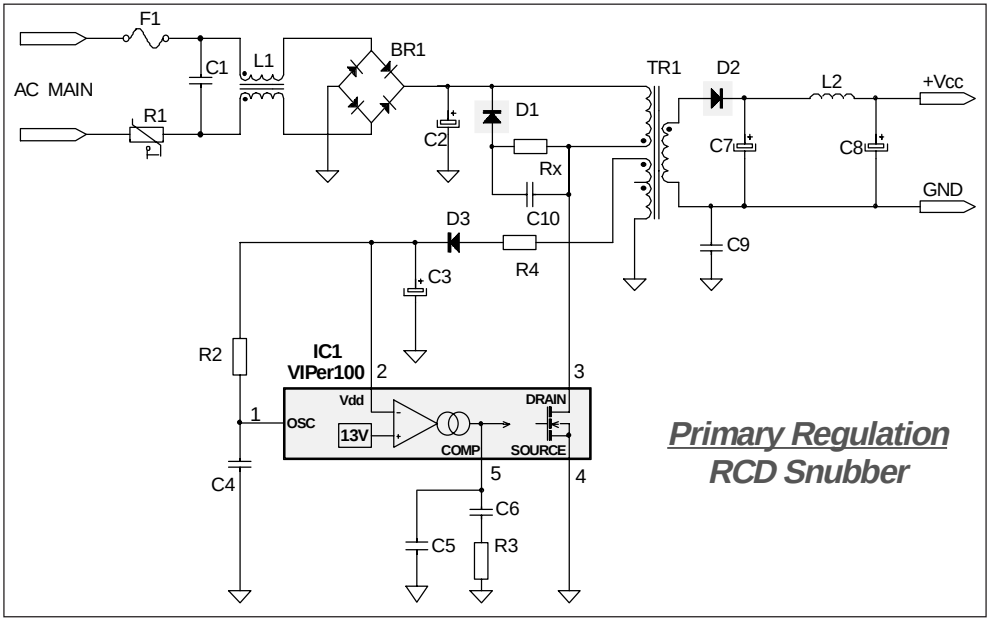
**Figure 3.** Off-Line Flyback SMPS with secondary regulation - Wide Voltage Input Range - 50W Power Output.




***Component List:***

F1 = 2A , 250VAC
L1 = RN114-2/02 SCHAFFNER
L2 = 1µH
C1 = 0.1µF, 400VAC
C2 = 150 µF, 400V
C3 = 47 µF, 16 V3.9nF, 200V
C4 = 4.7nF
C5 = 68 nF
C6 = 1 µF, 10V
C7 = 2,200+1,000 mF - 16V, EKR
C8 = 470µF - 16V, EKR
C9 = 1nF - 400V Class Y
C10 = 5.6nF - 200V
Cx = 100nF
BR1 = 400V, 1A
D1 = BYT11-600
D2 = BYW81-100
D3 = 1N4448
IC1 = VIPer100
IC2 = TL431
ISO1 = 4N25
R1 = 20$\Omega$
R2 = 5.6K$\Omega$, 1/8W
R3 = 1K$\Omega$, 1/8W
R4 = 10$\Omega$, 1/8W
R5 = 4.7K$\Omega$, 1/8W
R6 = 82K$\Omega$, 1/8W
R7 = 18K$\Omega$, 1/4W
R8 = 1.2K$\Omega$, 1/4W
Rx =2.2K$\Omega$
T1 = Transformer
$L_P$ = 150µH
$N_P/N_S$ = 7.83 (See Transformer section)

**Figure 4.** Off-Line Flyback SMPS with primary regulation, Wide Input Voltage Range, 50W Power Output

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C3 = 47 µF, 16 V3.9nF, 200V

C4 = 4.7nF

C5 = 18 nF

C6 = 560nF

C7 = 2,200+1,000 µF - 16V, EKR

C8 = 470µF - 16V, EKR

C9 = 1nF - 400V Class Y

C10 = 5.6nF - 200V

BR1 = 400V, 1A

D1 = BYT11-600

D2 = BYW81-100

D3 = 1N4448

IC1 = VIPer100

R1 = 20Ω

R2 = 5.6KΩ, 1/8W

R3 = 3.9KΩ, 1/8W

R4 = 10Ω, 1/8W

Rx = 2.2KΩ

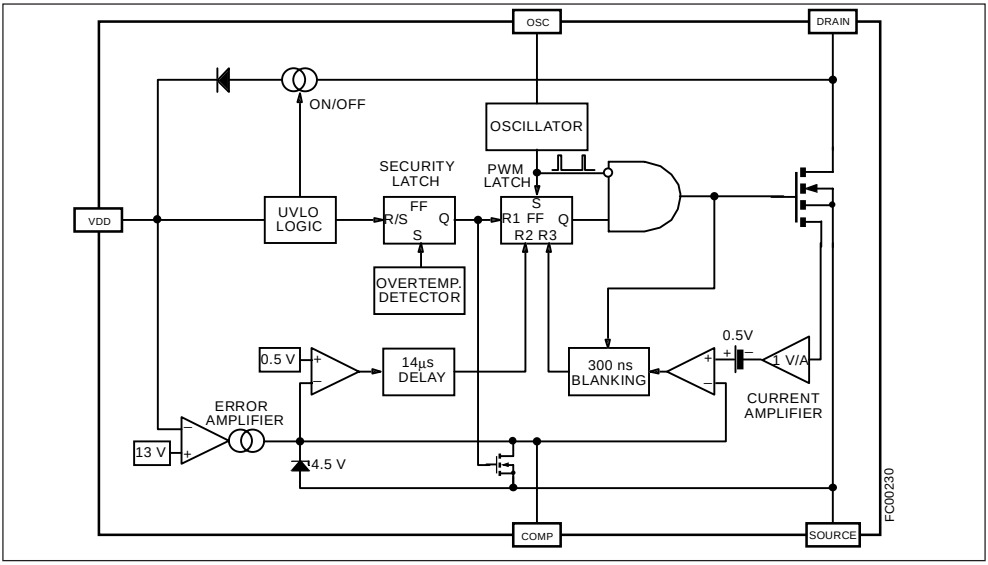
T1 = Transformer

$L_P$ = 150µH

$N_P/N_S$ = 7.83 (See Transfomer section)

## VIPerXXX FAMILY PINS FUNCTIONAL DESCRIPTION:

**Figure 5.** VIPer100™ - Internal Block Diagram




* **Drain pin :**

Integrated power MOSFET drain pin. It provides internal bias current during start-up via an integrated high voltage current source which is switched off during normal operation.The device is able to handle an unclamped current during its normal operation, assuring self protection against voltage surges, PCB stray inductance, and allowing a snubberless operation for low output power.

* **Source pin :**

Power MOSFET source pin. Primary side circuit common ground connection.

* **$V_{DD}$ pin :**

This pin provides two functions :

It corresponds to the low voltage supply of the control part of the circuit. If $V_{DD}$ goes below 8V, the start-up current source is activated and the output power MOSFET is switched off until the Vdd voltage reaches 11V. During this phase, the internal current consumption is reduced, the $V_{DD}$ pin is sourcing a current of about 1mA and the COMP pin is shorted to ground. After that, the current source is shut down, and the device tries to start up by switching again.

This pin is also connected to the error amplifier, in order to allow primary as well as secondary regulation configurations. In case of primary regulation, an internal 13V trimmed reference voltage is used to maintain $V_{DD}$ at 13V. For secondary regulation, a voltage between 8.5V and 12.5V will be put on $V_{DD}$ pin by transformer design, in order to stick the output of the transconductance amplifier to the high state. The COMP pin behaves as a constant current source, and can easily be connected to the output of an optocoupler. Note that any overvoltage due to regulation loop failure is still detected by the error amplifier through the Vdd voltage, which cannot surpass 13V. The output voltage will be somewhat higher than the nominal one, but still under control.

* **Comp pin** :

This pin provides two functions :

It is the output of the error transconductance amplifier, and allows for the connection of a compensation network to provide the desired transfer function of the regulation loop. Its' bandwidth can be easily adjusted to the needed value with the usual components value.

As stated above, secondary regulation configurations are also implemented through the COMP pin.

When the COMP voltage goes below 0.5V, the shut-down of the circuit occurs, with a zero duty cycle for the power MOSFET. This feature can be used to switch off the converter, and is automatically activated by the regulation loop (whatever the configuration) to provide a burst mode operation in case of negligible output power or open load condition.

* **Osc pin :**

An $R_T$-$C_T$ network must be connected on that pin to define the switching frequency. Note that despite the connection of $R_T$ to $V_{DD}$, no significant frequency change occurs for $V_{DD}$ varying from 8V to 15V. It provides also a synchronisation capability, when connected to an external frequency source.

For $R_T$ > 1.2 K$\Omega$ the switching frequency can be calculated as:

$$F_{sw} = \frac{2.3}{R_T \bullet C_T} \bullet D_{MAX}$$

$$D_{MAX} = 1 - \frac{550}{R_T - 150}$$

where the recommended oscillator Duty Cycle at $F_{SW}$ = 100KHz is: $D_{MAX}$ > 80%.

**Figure 6.** Switching frequency versus $R_T$ for different values of $C_T$

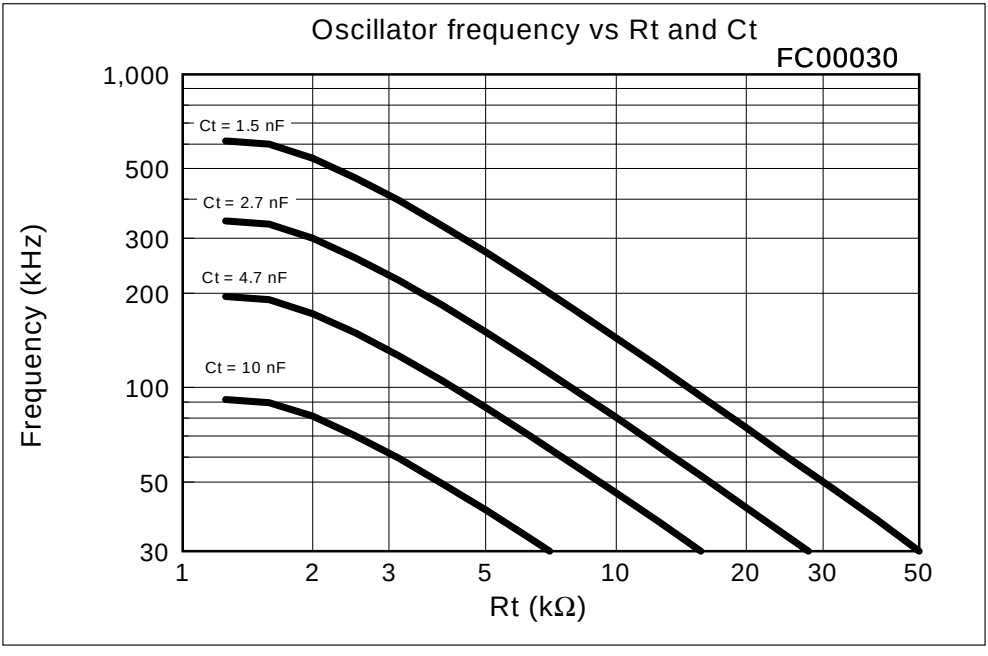
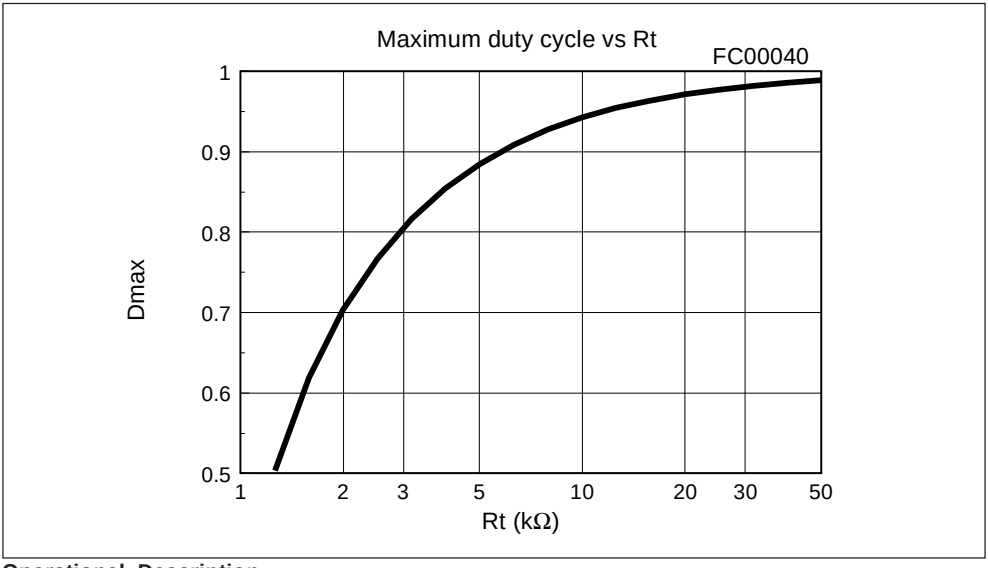


**Figure 7.** Maximum Duty Cycle Versus $R_T$




**Operational Description:**

**Current mode topology :**

The current mode control method, like the one integrated in the VIPer100/100A uses two control loops - an inner current control loop and an outer loop for voltage control. When the Power MOSFET output transistor is on, the inductor current (primary side of the transformer) is monitored with the SenseFET technique and converted into a voltage Vs proportional to this current. When Vs reaches VCOMP (the amplified output voltage error) the power switch is switched off. Thus, the outer voltage control loop defines the level at which the inner loop regulates peak current through the power switch and the primary winding of the transformer.

Excellent open loop D.C. and dynamic line regulation is ensured due to the inherent input voltage feedforward characteristic of the current mode control. This results in an improved line regulation, instantaneous correction to line changes and better stability for the voltage regulation loop.

Current mode topology also ensures good limitation in the case of short circuit. During a first phase the output current increases slowly following the dynamic of the regulation loop. Then it reaches the maximum limitation current internally set and finally stops because the power supply on $V_{DD}$ is no longer correct.

For specific applications the maximum peak current internally set can be overridden by externally limiting the voltage excursion on the COMP pin.

An integrated blanking filter inhibits the PWM comparator output for a short time after the integrated Power MOSFET is switched on. This function prevents anomalous or premature termination of the switching pulse in the case of current spikes caused by primary side capacitance or secondary side rectifier reverse recovery time.

**Stand-by Mode :**

Stand-by operation in nearly open load condition automatically leads to a burst mode operation allowing voltage regulation on the secondary side. The transition from normal operation to burst mode operation happens for a power Pstby given by :

$$P_{STBY} = ½ \cdot L_P \cdot I^2_{STBY} \cdot F_{SW}$$

where :

$L_P$ is the primary inductance of the transformer.

$F_{SW}$ is the nominal switching frequency.

$I_{STBY}$ is the minimum controllable current, corresponding to the minimum on time that the device is able to provide in normal operation. This current can be computed as :

$$I_{STBY} = \frac{(tb + td) \times V_{IN}}{L_P}$$

tb + td is the sum of the blanking time and of the propagation time of the internal current sense and comparator, and represents roughly the minimum on time of the device. Note that $P_{STBY}$ may be affected by the efficiency of the converter at low load, and must include the power drawn on the primary auxiliary voltage.

As soon as the power goes below this limit, the auxiliary secondary voltage starts to increase above the 13V regulation level forcing the output voltage of the transconductance amplifier to low state ($V_{COMP} < V_{COMPth}$). This situation leads to the shutdown mode where the power switch is maintained in the off state, resulting in missing cycles and zero duty cycle. As soon as $V_{DD}$ gets back to the regulation level and the $V_{COMPth}$ threshold is reached, the device operates again. The above cycle repeats indefinitely, providing a burst mode of which the effective duty cycle is much lower than the minimum one when in normal operation. The equivalent switching frequency is also lower than the normal one, leading to a reduced consumption on the input main lines.

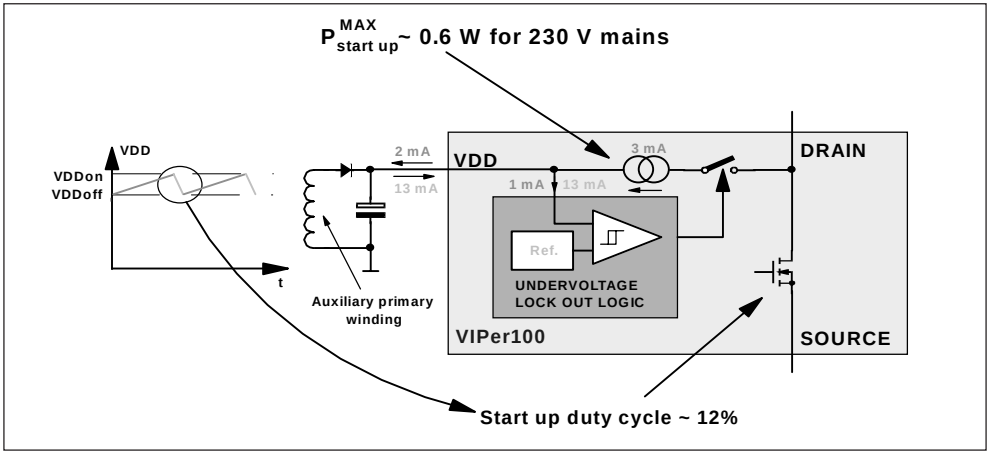
This mode of operation allows the VIPerXX0 devices to meet the new German “Blue Angel” Norm with less than 1W total power consumption for the system when working in stand-by mode. The output voltage remains regulated around the normal level, with a low frequency ripple corresponding to the burst mode.

The amplitude of this ripple is very low (< 10mV RMS), because of the output capacitors and of the low output current drawn in such conditions. The normal operation resumes automatically when the power get back to higher levels than Pstby.

**High Voltage start-up Current Source :**

An integrated high voltage current source provides a bias current from the DRAIN pin during the start-up phase. This current is partially absorbed by internal control circuits which are placed into a standby mode with reduced consumption and also provided to the external capacitor connected to the $V_{DD}$ pin. As soon as the voltage on this pin reaches the high voltage threshold $V_{DDon}$ of the UVLO logic, the device turns into active mode and starts switching. The start up current generator is switched off, and the converter should normally provide the needed current on the $V_{DD}$ pin through the auxiliary winding of the transformer, as shown in figure 8.

**Figure 8.** Behaviour of the high voltage current source at start-up



In case of an abnormal condition where the auxiliary winding is unable to provide the low voltage supply current to the $V_{DD}$ pin (i.e. short circuit on the output of the converter), the external capacitor discharges itself down to the low threshold voltage $V_{DDoff}$ of the UVLO logic, and the device goes back to the inactive state where the internal circuits are in standby mode and the start up current source is activated. The converter enters an endless start up cycle, with a start-up duty cycle defined by the ratio of charging current towards discharging when the VIPerXX0 device tries to start.

This ratio is fixed by design from 2 to 15, which gives a 12% start up duty cycle while the power dissipation at start up is approximately 0.6W, for a 230Vrms input voltage.

This low value of start-up duty cycle prevents the stress of the output rectifiers and of the transformer when in short circuit.

The external capacitor $CV_{DD}$ on the $V_{DD}$ pin must be sized according to the time needed by the converter to start up, when the device starts switching. This time tss depends on many parameters, among them which transformer design, output capacitors, soft start feature and compensation network implemented on the COMP pin.

The following formula can be used for defining the minimum capacitor needed :

$$CV_{DD} > \frac{I_{DD} \bullet t_{ss}}{V_{DDhys}}$$ where:

$I_{DD}$ is the consumption current on the $V_{DD}$ pin when switching. Refer to specified $I_{DD1}$ and $I_{DD2}$ values.

$t_{SS}$ is the start up time of the converter when the device begins to switch. Worst case is generally at full load.

$V_{DDhys}$ is the voltage hysteresis of the UVLO logic. Refer to the minimum specified value.

Soft start feature can be implemented on the COMP pin through a simple capacitor which will be also used as the compensation network.

In this case, the regulation loop bandwidth is rather low, because of the large value of this capacitor. In case a large regulation loop bandwidth is mandatory, the schematics of figure 9 can be used.

It mixes a high performance compensation network together with a separate high value soft start capacitor. Both soft start time and regulation loop bandwidth can be adjusted separately.

If the device is intentionally shut down by putting the COMP pin to ground, the device is also performing start-up cycles, and the $V_{DD}$ voltage is oscillating between $V_{DDon}$ and $V_{DDoff}$.

This voltage can be used for supplying external functions, provided that their consumption doesn't exceed 0.5mA.

Figure 10 shows a typical application of this function, with a latched shut down. Once the "Shutdown" signal has been activated, the device remains in the off state until the input voltage is removed.

**Figure 9.** Mixed Soft Start and Compensation

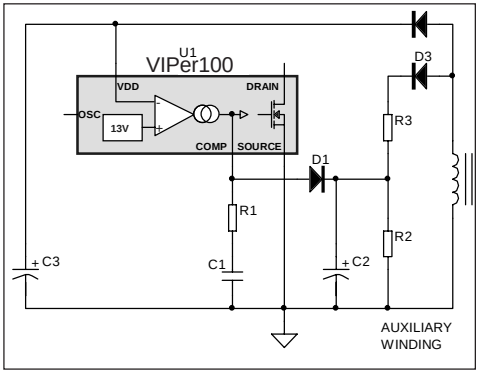
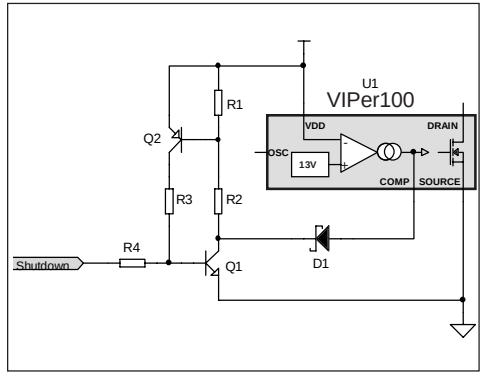



**Figure 10.** Latched Shut Down



**Transconductance Error Amplifier**

The VIPer100/100A includes a transconductance error amplifier. Transconductance Gm is the change in output current ($I_{COMP}$) versus change in input voltage (VDD). Thus:

$$G_M = \frac{\partial I_{COMP}}{\partial V_{DD}}$$

The output impedance $Z_{COMP}$ at the output of this amplifier (COMP pin) can be defined as :

$$Z_{COMP} = \frac{\partial V_{COMP}}{\partial I_{COMP}} = \frac{1}{G_m} \times \frac{\partial V_{COMP}}{\partial V_{DD}}$$

This last equation shows that the open loop gain AVOL can be related to Gm and $Z_{COMP}$ :

$$A_{VOL} = G_m \times Z_{COMP}$$

where the Gm value for VIPer100™ is typically 1.5 mA/V.

Gm is well defined by specification, but ZCOMP and therefore AVOL are subject to large tolerances. An impedance Z can be connected between the COMP pin and ground in order to define more accurately the transfer function F of the error amplifier, according to the following equation, very similar to the one above :

$$F(s) = G_m \times Z(s)$$

The error amplifier frequency / phase response is reported in figures 11 and 12 for different values of a simple resistance connected on the COMP pin. The unloaded transconductance error amplifier shows an internal $Z_{COMP}$ of about 330 KΩ.

**Figure 11.** Error Amplifier Frequency Response

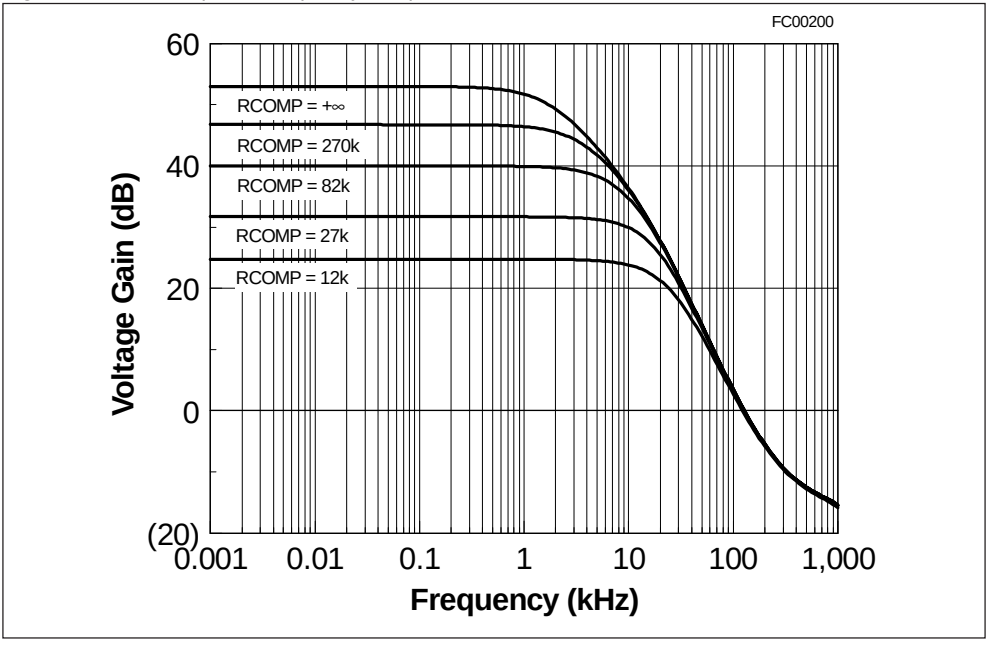
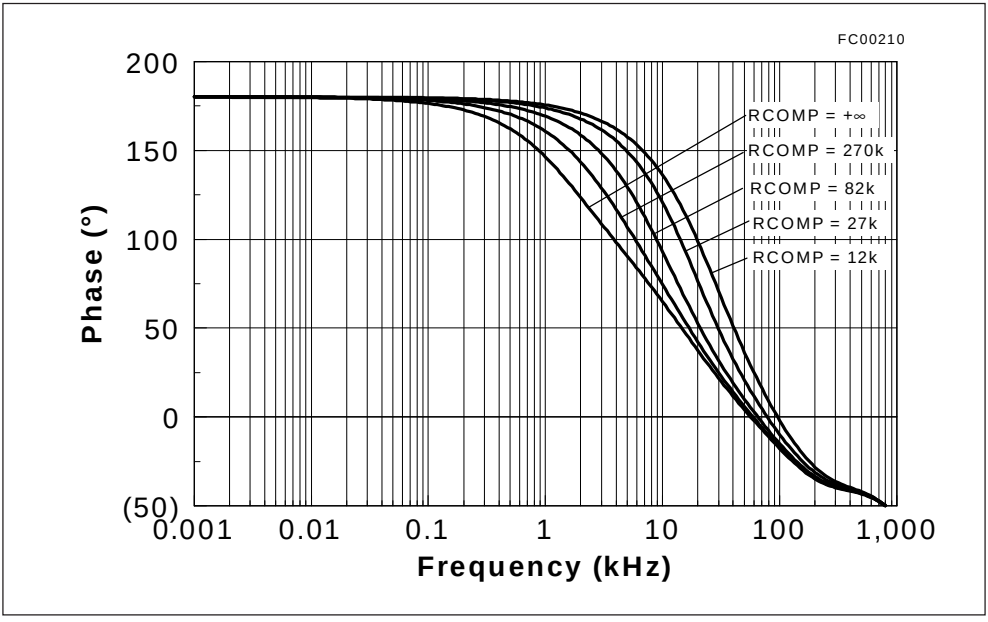


**Figure 12.** Error amplifier Phase response



More complex impedance can be connected on the COMP pin to achieve different compensation laws. A capacitor will provide an integrator function, thus eliminating the DC static error, and a resistance in series leads to a flat gain at higher frequency, insuring a correct phase margin. This configuration is illustrated in figure 13.

**Figure 13.** Typical compensation network.

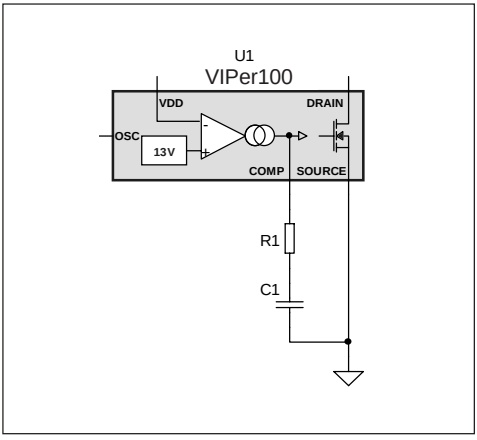
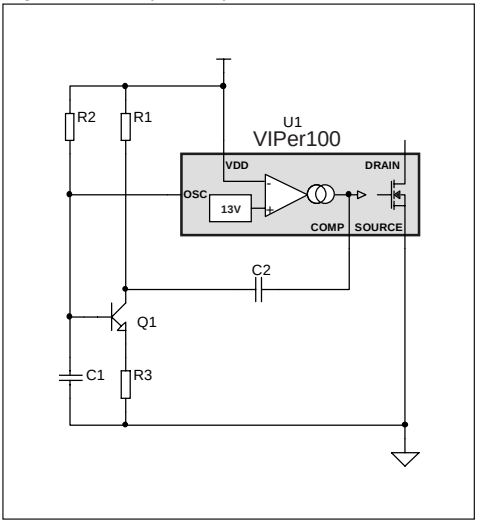



**Figure 14.** Slope compensation



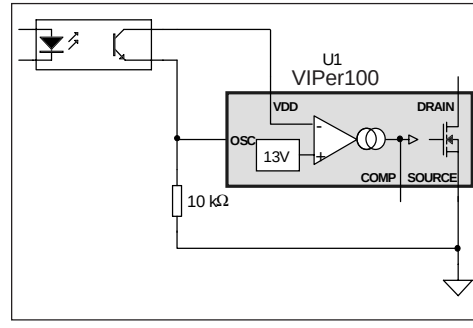

It is interesting to implement a slope compensation when working in continuous mode with a duty cycle higher than 50%. Figure 14 shows such a configuration. Note that R1 and C2 build the classical compensation network, and Q1 is injecting the slope compensation with the correct polarity from the oscillator sawtooth.

**External Clock Synchronization:**

The OSC pin provides a synchronisation capability, when connected to an external frequency source.

Figure 15 shows one possible schematic to be adapted depending the specific needs. If the proposed schematic is used, the pulse duration must be kept at a low value (500ns is sufficient) for minimizing consumption. The optocoupler must be able to provide 20mA through the optotransistor.

**Figure 15.** External clock synchronization




**Primary Peak Current limitation:**

The primary $I_{DPEAK}$ current and, as resulting effect, the output power can be limited using the simple circuit shown in figure 16. The circuit based on Q1, R1 and R2 clamps the voltage on the COMP pin in order to limit the primary peak current of the device to a value:

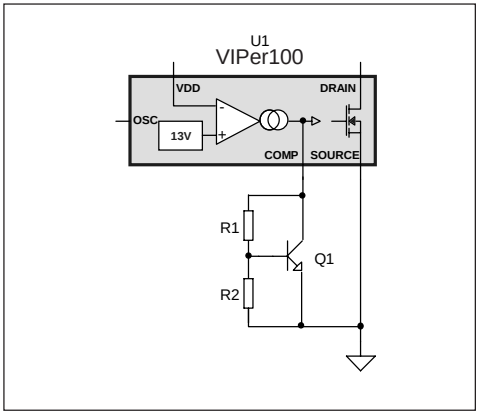
where:

$$I_{Dpeak} = \frac{(V_{COMP} - 0.5)}{H_{ID}}$$

$$V_{COMP} = 0.6 \times \frac{R1 + R2}{R2}$$

The suggested value for R1+R2 is in the range of 220Kohm.

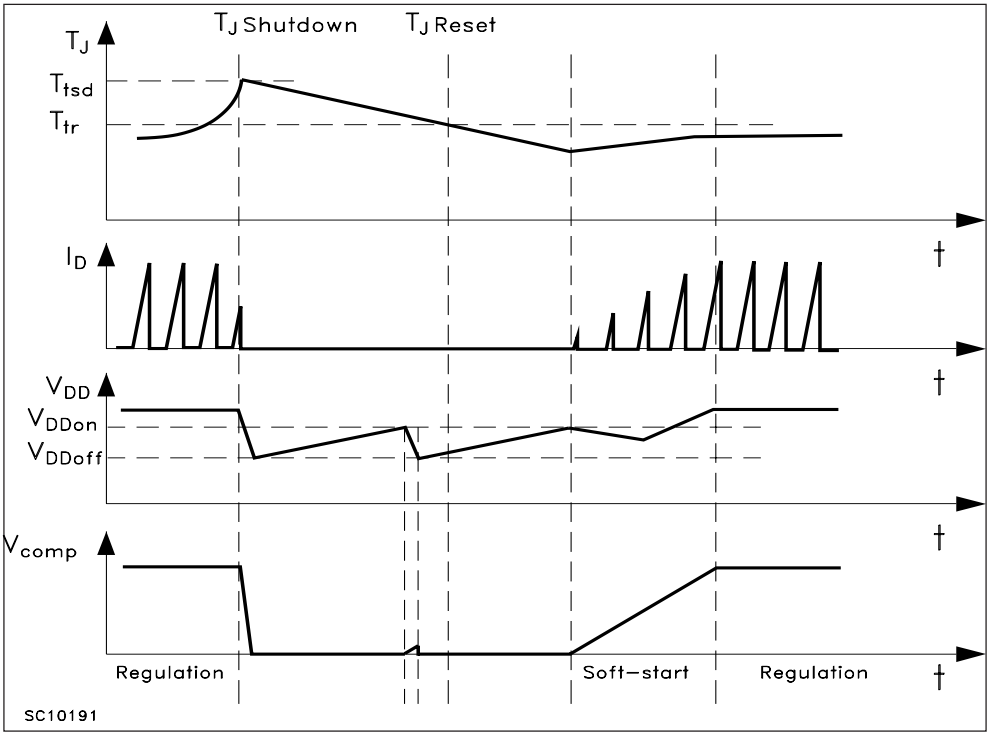
**Figure 16.** Output Power limitation




**Over-temperature protection:**

Over-temperature protection is based on chip temperature sensing. The minimum junction temperature at which over-temperature cut-out occurs is 140 °C while the typical value is 160 °C. The device is automatically restarted when the junction temperature decreases to the restart temperature threshold that is typically 22 °C below the shutdown value (see figure 17).

**Figure 17.** Sequence of operation in the case of thermal shutdown.



**Design Guidelines:**

With reference to the two schematics shown in figures 3 and 4, the basic design guidelines are given hereafter. This procedure can be easily adapted to modify the circuit according specific needs. The same procedures were applied for a Windows based design software.

**Topology:**

*Flyback Converter operating in the discontinuous inductor current mode.*

In the discontinuous inductor current mode all the energy stored in the primary inductance of the flyback transformer must be zero at the end of each switching cycle. During the on time, all the energy taken from the input is stored in the transformer according the equation $\mathbf{E=1/2LI_P^2}$. When the output Power MOSFET is switched off , the stored energy is for a major part delivered to the load and for a part is dissipated on the primary side because of the undesiderable leakage inductance. The power output to the load is equal to the energy stored in the inductance times the frequency and the efficiency: $\mathbf{P_{OUT}=\eta*1/2LI_p^2*f_{SW}}$. To assure discontinous operation and core reset, the Volt*second product across the primary of the transformer during reset must be equal or exceeding the Volt*second applied during the on time of the Power MOSFET output stage:

$$V_{FL} \cdot t_{reset} \geq V_{IN(min)} \cdot t_{on}$$

**Input Section:**

A standard input line filter, to reduce EMC down the maximum allowable value, is obtained with C1 and L1, and also with the common mode capacitor C9.

AC line voltage is rectified and filtered by the full bridge BR1 and C2 in order to create a high-voltage DC ranging - in the case of a wide input voltage range - from 120 to 380VDC. The value of C2 is determined by fixing the minimum input voltage for the converter circuit at full load, fixed to $V_{MIN}$=70V for this example. The worst case condition is fixed by the minimum line voltage of 85VAC, 50Hz. In this situation we have:

RMS line voltage = $I_{RMS}$ = 85VAC

Peak no-load voltage on filter capacitor = $V_{PEAK}$ = 120V

Capacitor voltage ripple at full load = $V_{ripple} = V_{PEAK} - V_{MIN}$ =120-70=50V

Since C2 must provide all energy requirement of the power supply during its discharge phase, the required energy for each charging phase (2 times for each line cycle) is:

$$W_{IN} = \frac{Power\_out}{Efficiency} \cdot T_D = \frac{50}{0.75} \cdot T_D$$

where $T_D$ is the discharging time of C2 at each half line cycle. It can be computed as

$$T_D = 5ms \cdot \left( 1 + \frac{\arcsin\left(\frac{V_{MIN}}{V_{PEAK}}\right)}{90} \right) = 7ms$$

and the capacitor value can be calculated from:

$$W_{IN} = \tfrac{1}{2} C_2 \left( V_{PEAK}^2 - V_{MIN}^2 \right) = 465mJ$$

Therefore :

$$C2 = \frac{2 \cdot W_{IN}}{V_{PEAK}^2 - V_{MIN}^2} = \frac{0.931}{120^2 - 70^2} =$$

$$= 98\mu F$$

In the application a standard value of 150µF, 400V is suggested which allows a good design margin and takes into account that the worst case condition for a standard electrolitic capacitor is $C_{MIN}$=($C_{NOMINAL}$.-20%) leading to a worst case value for $C2_{MIN}$ of 120µF.

According to this definitive value for $C2_{MIN}$, the new discharging time of C2 can be computed as the solution of the equation :

$$\sqrt{V_{PEAK}^2 - \frac{2 \cdot Power\_out \cdot T_D}{\eta \cdot C2_{MIN}}} =$$

$$= V_{PEAK} \cdot \sin\left(\omega \cdot T_D - \frac{\pi}{2}\right)$$

successive approximation with a dichotomic method.

With the above values, $T_D$ is about 7.3ms. $V_{MIN}$ can now be computed

$$V_{MIN} = V_{PEAK} \cdot \sin\left(\omega \cdot T_D - \frac{\pi}{2}\right) =$$

$$= 120 \cdot \sin\left(2 \cdot \pi \cdot 50 \cdot 0.0073 - \frac{\pi}{2}\right) =$$

$$= 79.6V$$

## Transformer

The aim of this paragraph is to calculate the primary inductance of the transformer and to fix all boundary design constraints including the core choice, turns calculation and windings AWG datas.

The maximum allowable duty cycle is defined by the breakdown capability of the output Power MOSFET ($BV_{DSS}$=600V min). At turn off the voltage across the power switch is $V_{DS}$ = VDCmax + Flyback voltage + Leakage inductance spike.

Since VDCmax is 380V, we can fix by design:

$V_{FL}$ = Flyback voltage = 100V

$V_{pp}$ = Leakage inductance spike = 600 - 380 - 100 = 120V

No margins are needed with respect to the breakdown voltage because of the avalanche capability of the device.

Under the above condition and for a minimum DC input voltage of 79.6V we can calculate the maximum duty cycle to stay in discontinuous mode operation,

$$D_{MAX} = \frac{V_{FL}}{(V_{MIN} - V_{TR}) + V_{FL}} =$$

$$= \frac{100}{79.6 + 100} = 55.7\%$$

Where $V_{TR}$ is the voltage drop on the MOSFET power stage at $I_{pk}$. For this example $V_{TR}$ = 0V.

The peak current on the primary inductance at full load ($P_0$=50W) and for a given ( $\eta$ = 0.75 ) is:

$$Ipk = \frac{2P_0}{\eta \bullet (V_{MIN} \bullet D_{MAX})} =$$

$$= \frac{100}{0.75 \bullet 79.6 \bullet 0.557} = 3.0A$$

The primary inductance can then be calculated as:

$$L_P = \frac{V_{MIN} \bullet D_{MAX}}{I'_{pk} \bullet F_{SW}} = \frac{79.6 \bullet 0.557}{3.0 \bullet 100000} =$$

$$= 0.147mH$$

The leakage inductance, $L_{pl}$ , can be assumed with good approximation equal to 5% of $L_p$ having

$$L_{pl} = 0.05 \bullet L_p = 7.3\mu H$$

A possible core selection for a similar transformer is the very common ETD29 core with a ferrite grade 3C85 that is able to work at $F_{SW}$ = 100KHz with acceptable core losses.

From the ETD29 datasheets we have:

* Effective Area $A_e = 76mm^2$;
* Suggested Flux density $B_{max}$ = 0.125T (to limit core losses);
* Average lenght of turn $L_{AVG}$ = 53mm.

The primary turns $N_P$ can be calculated as:

$$N_P = \frac{L_P \bullet I_{pk}}{B_{MAX} \bullet A_e \bullet 10^{-6}} = \frac{147 \bullet 10^{-6} \bullet 3.0}{0.125 \bullet 76 \bullet 10^{-6}} = 47$$

The power secondary turns $N_{spower}$ can be calculated as:

$$N_{SPOWER} = \frac{N_P \bullet (V_{out} + V_{diode})}{V_{FL}} =$$

$$= \frac{47 \bullet (12 + 0.7)}{100} = 6$$

and for primary regulation,

$$N_{Paux} = \frac{N_P \bullet (13 + V_{diode})}{V_{FL}} = \frac{47 \bullet 13.7}{100} = 6.44$$

while for secondary regulation,

$$N_{Saux} = \frac{N_P \bullet (11 + V_{diode})}{V_{FL}} = \frac{47 \bullet 11.7}{100} = 5.50$$

The air gap can be calculated as,

$$A_G = \frac{4\Pi \bullet N_P \bullet I_{pk}}{B_{MAX} \bullet 10^4} = \frac{4\Pi \bullet 47 \bullet 3.0}{0.125 \bullet 10^4} = 1.42mm$$

At this point it is possible to choice the copper section for primary and secondary windings. Under the condition to accept 1W copper lossess in the worst case condition we can easily calculate the theoretical copper section. Our simplified choice is to split the losses between the primary and the secondary windings (0.5+0.5W) and to use several wires of little section paralleled together.

. This in order to minimize the skin effect or penetration depth (0.024cm @ 100KHz) otherwise resulting in un-acceptable AC resistance.

Taking as example the primary winding and considering 0.5W total copper losses we can calculate the resulting allowable resistance:

$$R_P = \frac{P_P}{I^2_{RMS}} = \frac{P_P}{I_{pk} \bullet \sqrt{(D_{MAX}/3)}} =$$

$$= \frac{0.5}{3.0 \bullet \sqrt{(0.556/3)}} = 0.3044\Omega$$

and considering that we have 47 turns with an average length of 53mm,

$$R_P/cm = \frac{R_P}{47 \bullet 5.3} = 0.00122\Omega/cm$$

, this resistance value can be achieved using 4 paralled AWG29 wires.

Withe the same procedure we can calculate for the power secondary winding that are needed 7 paralleled AWG24 wires.

**Snubbing Circuit:**

The network **D1, Rx, C10** limits the voltage spike at turn-off caused by the leakage inductance $L_{pl}$ of the power transformer T1. The energy stored in the leakage inductance, is transferred to the capacitor C10 which is dimensioned according the following equation (taking into consideration that capacitor has a residual voltage egual to $V_{fl}$ at turn off).

$$C10 = \frac{L_{pl} \bullet I^2_{pk}(max)}{V^2_{pp}}$$

where:

$L_{pl}$= Leakage inductance = 7.3 µH ;

$V_{pp}$ = Allowable Voltage spike due to leakage inductance = 120V for this example

$$C10 = \frac{7.3 \bullet 10^{-6} \bullet 3^2}{120^2} = 0.00477\mu F \cong 5.6nF$$

The resistor Rx is calculated under the hypothesis to discharge C10 during a period leaving a residual voltage of $V_{fl}$ at the time of the next turn-off.

$$Rx = \frac{T}{C10 \bullet \ln\left(1 + \frac{V_{PP}}{V_{FL}}\right)} =$$

$$= \frac{10 \bullet 10^{-6}}{5.6 \bullet 10^{-9} \bullet \ln\left(1 + \frac{120}{100}\right)} = 2289\Omega = 2.2k\Omega$$

The power dissipated in Rx is the energy discharged from C10 times the switching frequency, here fixed by design to 100KHz :

$$P_d = ½ \bullet C10 \bullet \left((V_{FL} + V_{PP})^2 - V^2_{FL}\right) \bullet f =$$

$$= 10.53W$$

This value is rather pessimistic because part of the leakage energy is absorbed by local parasitic capacitance, and an another part is restituted back to the secondary side because of the recovery time of the diode D1. The computed values here above gives a first guess of what could be the sizing of the snubber. Practical measurements will provide the final components choice.

Another topology can be used for clamping the voltage on the drain of the device, with transil. Suited types (1.5KExxx or BZW80/xxx) are available from ST, and offers good operation in every condition (input voltage and/or output power variations). Particular care should be taken to the design of the snubber circuit, when low mains power is required in converter stand by mode. In this case, the transil device is definitively the better one.

**Output Filter:**

The network **C7+C7', L2, C8** in figure 4, provides filtering of the output voltage to meet the output ripple specification. To calculate the capacitors values it is necessary to consider that these components are not ideal. Each capacitor has resistance $R_0$ and inductance $L_0$ in series. These are referred to as the *equivalent series resistance* (**ESR**) and *equivalent series inductance* or (**ESL**).

Up to 200KHz operation $L_0$ can be neglected for the output ripple determination.

This means that we have two ripple components due to $R_0$ and $C_0$ not in phase. For a worst case comparison, however, it can be assumed that they are in phase.

From the practical point of view it is possible to demonstrate that to calculate the capacitor value it is enough to calculate the ESR value for having a certain output ripple and choose in the capacitor catalogue that value of capacitor that shows the needed ESR at the switching frequency. More commonly, it is possible to find in the catalogues the value $R_0{*}C_0$ [$\Omega$*µF].

If we need to have a voltage ripple, $V_{07pp}$, of 0.50V across C7 we can calculate:

$$ESR_{C7} = R_{07} = \frac{V_{07pp}}{I_{Spk}}$$

Where:

$$I_{Spk} = \frac{2 \bullet I_{out}}{(1 - D_{max})} = \frac{2 \bullet 4.16}{(1 - 0.557)} = 18.80A$$

Therefore:

$$ESR_{C7} = R_{07} = \frac{0.50}{18.80} = 0.027\Omega$$

Considering that an average quality capacitor suitable for 100KHz operation shows a value $R_0{*}C_0$ = 65 [$\Omega$*µF] , we can calculate :

$$C_{07} = C_7 = \frac{65}{0.019} = 2{,}445\mu F$$

For the real application are used two capacitor in parallel (C7 and C7') respectively of 2,200µF and 1,000µF, 16V.

In order to further reduce the output ripple it is possible to add an additional L-C filter. In our example we need a ripple value across C8 (and the load) of $V_{08pp}$=0.10V.

For 100KHz operation a practical value of 1mH can be used for the series inductance. At 100KHz operation 1mH inductance leads to a resistance of $R_{L2}$=0.63$\Omega$.

Once again we can consider that the main source for the ripple on C8 is the ESR of the capacitor. If we consider the equivalent circuit showing only the resistive components of L2 and C8 at 100KHz, we can calculate $ESR_{C8}$:

$$ESR_{C8} = R_{08} = \frac{V_{08pp} \bullet R_{L2}}{V_{07pp} - V_{08pp}} = \frac{0.1 \bullet 0.63}{0.5 - 0.1} =$$

$$= 0.16\Omega$$

Therefore:

$$C_{08} = \frac{65}{0.16} = 414\mu F$$

The value used in the application is C8 =470µF.

The same results apply also to figure 3 where: C7 = 2,200µF, C7' = 1,000µF, L2 = 1µH, C8 = 470µF.

**Closing the Feedback loop:**

The objective of this paragraph is to give guidelines to design a closed-loop negative feedback system around the **VIPer100™**. As shown in the next figure, the closed loop feedback system can be described in terms of 3 major elements:

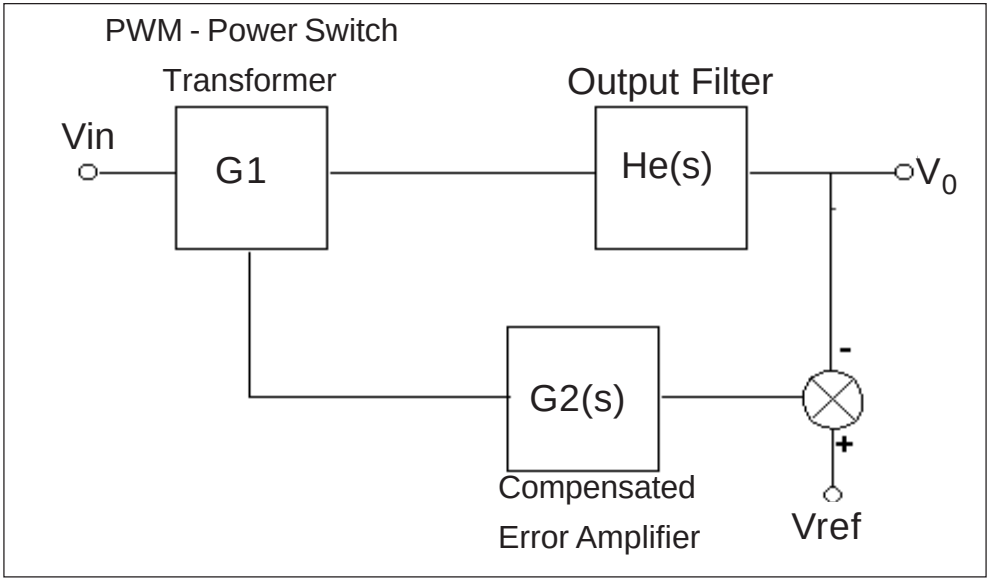
G1: PWM, Integrated Power MOSFET and Transformer;

G2(s): Error amplifier and Compensation Network;

He(s): Output filter.

The gain loop parameters (gain and phase shift) can be represented using Bode plots. Since G1 and He(s) are predetermined by the application and the circuit topology, the task in closing the feedback loop is to define the characteristics of the error amplifier (if external) and related compensation network, G2(s), that results in the optimum closed loop gain-bandwidth for good dynamic response, line and load regulation and stability.

**Figure 18.** Control loop block diagram




A common approach to design the desired closed loop characteristic is the following:

1) Represent the Bode plot of the transfer function G1*He(s);

2) Define the optimum transfer characteristic to achieve good dynamic response, line and load regulation and stability;

3) Design the compensation network G2(s) in such a way that the sum of the gain of G2(s) and G1*He(s), matches the transfer characteristic defined at point 2.The phase margin must be verified as well.

At this point we need to know how to calculate the tranfer functions G1*He(s). We can make the following considerations:

$$I_{pk} = K \bullet V_{COMP} \quad (1), \; P_0 = \frac{V_0^2}{R_0} \quad (2),$$

$$P_0 = \tfrac{1}{2} \bullet L_P \bullet I_{pk}^2 \bullet f \bullet \eta \quad (3)$$

where $K=1/H_{ID}$

And combining (1), (2) and (3)

$$V_0 = \sqrt{\frac{L_P \bullet I_{PK}^2 \bullet R_0 \bullet f \bullet \eta}{2}} =$$

$$= I_{PK} \bullet \sqrt{\frac{L_P \bullet R_0 \bullet f \bullet \eta}{2}} =$$

$$= K \bullet V_{COMP} \sqrt{\frac{L_P \bullet R_0 \bullet f \bullet \eta}{2}}$$

Thus, considering also the power transformer turns ratio n=Np/Ns, and that the values of primary inductance, filter capacitance and load resistance must be referred into the output we are monitoring according their respective turns ratios squared,

$$G1 = \frac{V_D}{V_{COMP}} = K \bullet n \bullet \sqrt{\frac{L'_P \bullet R'_0 \bullet f \bullet \eta}{2}} =$$

$$= \frac{1}{H_{ID}} \bullet \sqrt{\frac{L_P \bullet R_0 \bullet f \bullet \eta}{2}} \quad (4)$$

And,

$$He(s) = \frac{1 + (s/\omega z))}{1 + (s/\omega p))}, \; P = \frac{1}{\Pi R'_0 C'_0} \quad (5),$$

$$Z = \frac{1}{2\Pi \bullet (ESR)' \bullet C'_0} \quad (6)$$

where (ESR'*C'$_0$) in formula (6) is the ($R_0$*$C_0$) in [$\Omega$*F] related to the used capacitors (for our example 65*10$^{-6}$ [$\Omega$*F] )

To underline that, as reported in formula (5), the effective power cell pole of a discontinuous flyback is the double of the one of the load itself, when this load is constituted of a filtering capacitor and the load resistor. The theoretical explanation and some experimental measurements are reported in Appendix A.

Primary Regulation:

In the case of the application in fig. 2 (primary regulation), we have:

K=1 (see VIPer100™ datasheet);

n = Np/Ns = 47/7 =6.7;

$C_0' = 47 + 3670*(6/7)^2 = 2743\mu F$;

$R_0' = (13)^2 / 50 = 3.38\Omega$ (min) ; $R'_0 = (13)^2 / 5 = 33.8\Omega$ (max);

Therefore,

$$G1 = 1\sqrt{\frac{147 \cdot 3.38 \cdot 0.1 \cdot 0.75}{2}} = 4 \cong 13dB$$

*at max load*

The pole frequency of the output filter capacitance and load resistance is:

$$p = \frac{1}{\Pi \cdot R_0' \cdot C'} = \frac{1}{3.14 \cdot 3.38 \cdot 0.002743} = 34Hz$$

The zero frequency of the output filter capacitance and associated ESR is:

$$Z = \frac{1}{2\Pi \cdot ESR' \cdot C'} = \frac{1}{6.28 \cdot 65 \cdot 10^{-6}} = 2{,}450Hz$$

The second step is to design the feedback transfer function G2(s) and to choose the values for the network **$R_3$ - $C_5$ -$C_6$**

The following procedure can be applied:

1)To fix a pole of G2(s) at the zero of G1*He(s);

2)To cross 0dB for the overall transfer function at 1/3 of the frequency where is located the zero of G1*He(s). The crossing frequency is named $f_{C0}$;

3)To fix a zero of G2(s) at 1/10 of $f_{C0}$;

Therefore,

$$f_{CO} = \frac{2450}{3} = 817Hz$$

$$G2(s)_{817Hz} = [(\log 817 - \log 34) \cdot 20 - 13] =$$

$$= 14.82dB$$

At this point, since we know $g_m$ = 1.5 mA/V, we can fix $R_3$

$R_3 \cdot g_m = 14.82dB$ resulting in:

$R_3 \cong 3.9K\Omega$

According the point 1), the pole of G2(s) is fixed by $C_6$'

$$C_5 = \frac{1}{2 \cdot \Pi \cdot 3.9 \cdot 10^3 \cdot 2450} \cong 18nF$$

(rounded to a commercial value)

According the point 3), the zero of G2(s) is fixed by $C_6$

$$C_6 = \frac{1}{2 \cdot \Pi \cdot 3.9 \cdot 10^3 \cdot 80} = 500nF \cong 560nF$$

An additional pole is added at very low frequency by $C_5$ in parallel to $C_6$ and the internal resistance of the COMP pin that is equal to 330K$\Omega$.

$$p = \frac{1}{2 \cdot \Pi \cdot 330 \cdot 10^3 \cdot 578 \cdot 10^{-9}} = 0.83Hz$$

The phase margin for the overall transfer function at $f_{C0}$ can be calculated as:

$$M(\phi) =$$

$$= 360^0 - 180^0 - tg^{-1}\left(\frac{817}{0.83}\right) - tg^{-1}\left(\frac{817}{34}\right) +$$

$$+ tg^{-1}\left(\frac{817}{80}\right) = 86.8^0$$

The same procedure can be repeated at min load (for this example 5W that leads to a $R'_0$=33.8$\Omega$

The gain Bode diagrams at max load and min load are represented in figures 19 and 20, while the phase Bode diagram for both cases is represented in figure 21.

**Figure 19.** Gain Bode Plot at Max Load

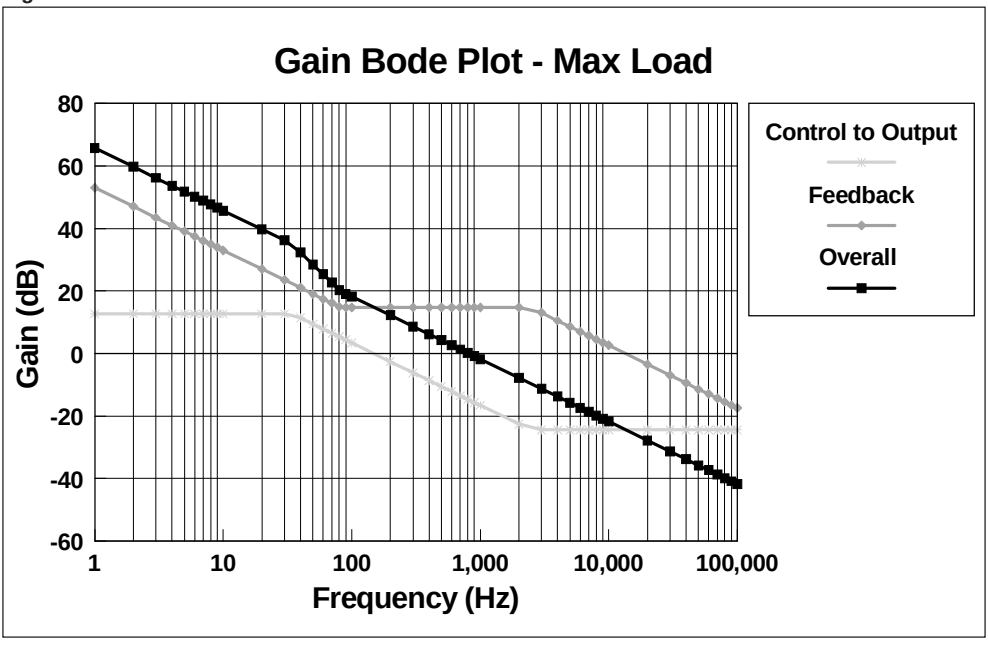



**Figure 20.** Gain Bode Plot at Min Load

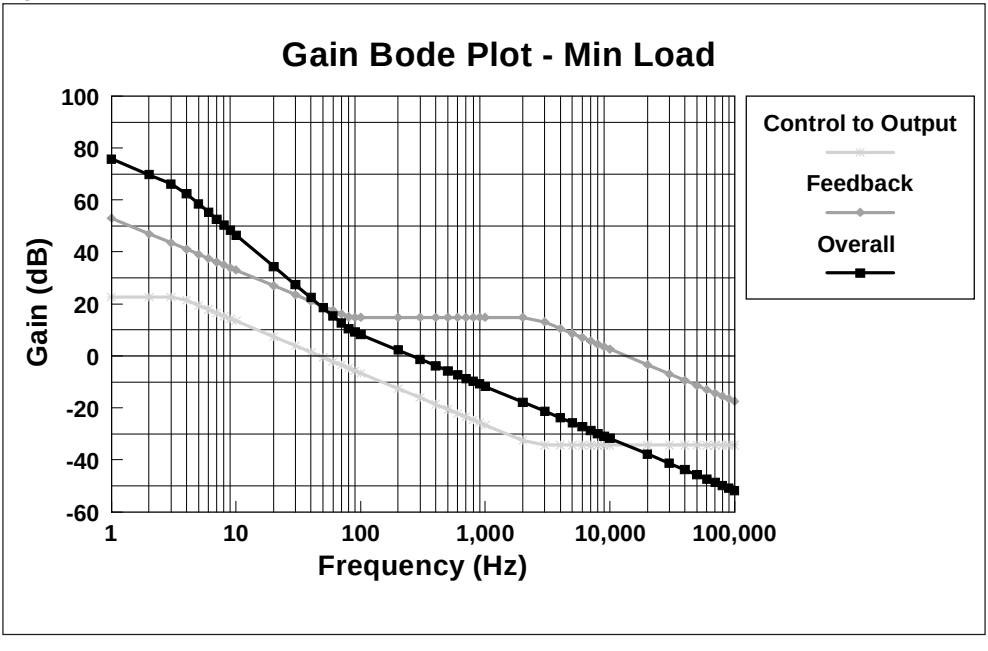
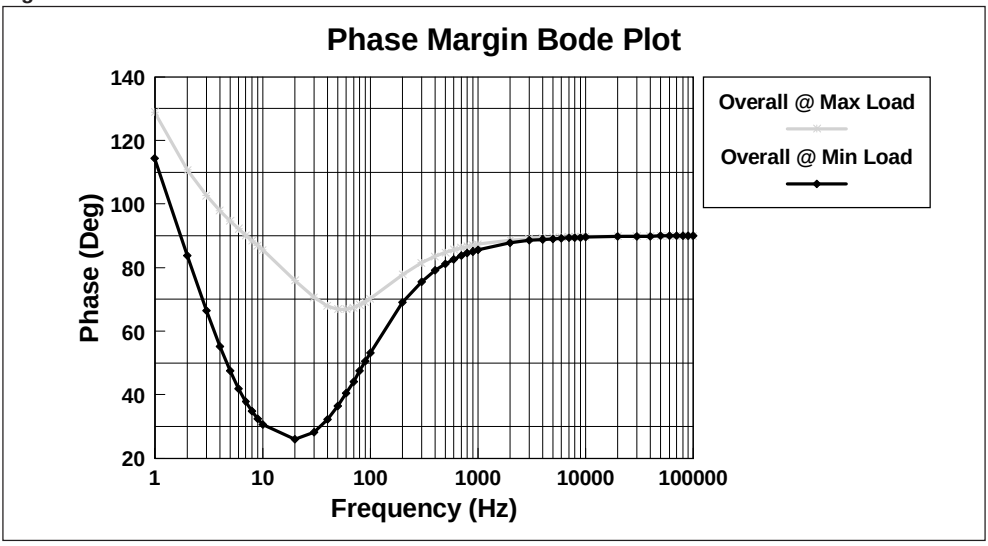


**Figure 21.** Phase Bode Plot



**Secondary Regulation:**

In the case of the application in fig. 1 (secondary regulation), we have:

K=1 (see VIPer100™ datasheet);

n = Np/Ns = 47/6 =7.83;

$C_0' = 3670 + 47*(5/6)^2 = 3{,}702\ \mu F$;

$R_0' = (12)^2 / 50 = 2.88\Omega$ (min) ; $R'_0 = (12)^2 / 5 = 28.8\Omega$ (max);

Therefore,

$$G1(s) = 1 \bullet \sqrt{\frac{147 \bullet 2.88 \bullet 0.1 \bullet 0.75}{2}} =$$

$$= 3.98 \cong 12dB \text{ } \textit{at max load}$$

Compensation network

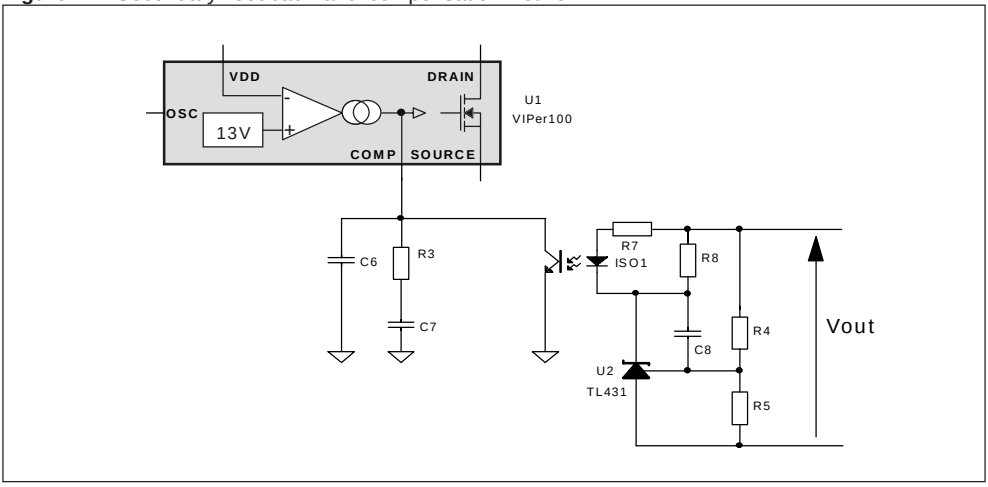
Built around R3, C5 and C6. Basically, it is possible to eliminate C5 and C6, but :

*C5 is needed because of noise filtering. It will be also used for setting a pole at the same place than the zero of the power cell, due to the ESR of the filtering output capacitor.

*In the general case, C6 will be used to build a soft start, because it is not really needed to provide the zero of the regulation loop. Its value will be in the range of a few mF, according to the following formula :

$$C_6 = \frac{I_{COMPHI} \bullet t_{SS}}{V_{COMP}^{NOM} - V_{COMPth}}$$ where :

**Figure 22.** Secondary feedback and compensation network




The pole frequency of the output filter capacitance and load resistance is:

$$p = \frac{1}{\Pi \bullet R_0' \bullet C'} = \frac{1}{3.14 \bullet 2.88 \bullet 0.003702} \cong$$

$$\cong 30Hz$$

The zero frequency of the output filter capacitance and associated ESR is:

$$Z = \frac{1}{2\Pi \bullet ESR' \bullet C'} = \frac{1}{6.28 \bullet 65 \bullet 10^{-6}} = 2{,}450Hz$$

The second step is to design the feedback transfer function G2(s) and to choose the value of all involved parts.

For a better understanding of the applied procedure some basic considerations should be considered with reference to figure 22.

$I_{COMPHI}$ and $V_{COMPth}$ are given in the VIPer100 or VIPer50 datasheeets (They do not depend on the type of VIPer).

$t_{SS}$ is the desired soft start time (Input parameter).

$V_{COMP}^{NOM}$ is the nominal voltage on the compensation pin when in steady state. It can be computed from the other parameters of the software with the following formula :

$$V_{COMP}^{NOM} = H_{ID} \bullet I_P + V_{COMPoff}$$

where :

$H_{ID}$ and $V_{COMPoff}$ are given in the VIPer100 or VIPer50 datasheeets (They do not depend on the type of VIPer).

$t_{SS}$ is the desired soft start time (Input parameter).

$V_{COMP}^{NOM}$ is the nominal voltage on the compensation pin when in steady state. It can be computed from the other parameters of the software with the following formula :

$$V_{COMP}^{NOM} = H_{ID} \bullet I_P + V_{COMPoff} \quad \text{where:}$$

$H_{ID}$ and $V_{COMPoff}$ are given in the VIPer100 or VIPer50 datasheeets ( $H_{ID}$ depends on the type of VIPer).

$I_P$ is the peak primary current in steady state.

As we have : $V_{COMPoff} \approx V_{COMPth}$ it comes :

$$C6 = \frac{I_{COMPHI} \bullet t_{SS}}{H_{ID} \bullet I_P}$$

R3 will always have the same value, we suggest 1k$\Omega$. This value avoids that at start up, the soft start function is hidden by too high an immediate voltage on the compensation pin ($I_{COMPHI} \bullet R_3$) and provides correct large signal dynamic behaviour in case of large output current changes.

According to this value, C6 will always have a minimum value of 1µF, in order to avoid any interference with the higher frequency poles and zeros of the overall regulation loop. This will be the value by default, if no soft start is needed, or if the desired soft start time leads to a lower value.

For our example, considering $t_{ss}$= 5msec, we have

$$C6 = \frac{600 \bullet 10^{-6} \bullet 5 \bullet 10^{-3}}{1 \bullet 3} = 1\mu F$$

that is also the minimum allowed value for this specific suggested compensation network.

**TL431 biasing**

R8 provides a supplementary biasing current for the TL431. This biasing current is the sum of the one delivered by R8 and the one needed by the diode of the optocoupler. A good characteristic of the VIPer family is that this current is fixed (When in steady state) and doesn't depend on the output load. Therefore, a simple formula can be used to compute the value of this resistance, with sufficient margin for the large signal dynamic behaviour :

$$R8 = \frac{V_{FB}^{ISO1} + R_6 \bullet \frac{I_{COMPHI}}{G^{ISO1}}}{I_B^{U2}}$$

where :

$I_{COMPHI}$ is given in the VIPer100 or VIPer50 datasheeets (It doesn't depend on the type of VIPer).

$V_{FB}^{ISO1}$ and $G^{ISO1}$ are respectively the forward voltage of the diode and the current gain of the optocoupler ISO1.

$I_B^{U2}$ is the needed biasing current of the TL431. It is about 1mA for classical devices. $R_6$ will be computed for loop stability purpose.

**TL431 and optocoupler transfer function**

The optocoupler diode current Id can be written as follows :

$$Id = \frac{V_{out} - F(s) \bullet V_{out}}{R_6} = \frac{1 - F(s)}{R_6} \bullet Vout$$

where F(s) is the transfer function of the TL431 and associated components.

We have : $F(s) = -\frac{1}{R_7 \bullet C_X \bullet s}$ and therefore :

$$Id = \frac{1}{R_6} \bullet \frac{1 + R_7 \bullet C_X \bullet s}{R_7 \bullet C_X \bullet s} \bullet Vout$$

Note that R5 never impacts on the small signal transfer function. It only sets the DC value of the output voltage. Its value can be fixed at 4.7k$\Omega$ and the one of R7 is defined accordingly :

$$R_7 = R_5 \bullet \left(\frac{Vout}{Vref} - 1\right) \quad \text{where:}$$

Vout is the desired output voltage.

Vref is the reference voltage of the used programmable zener. Either 2.5V (The most conventional) or 1.25V (For micropower models).

For our example, considering a standard TL431 and $V_{out}$=12V, we have:

$$R_7 = 4.7 \bullet \left(\frac{12}{2.5} - 1\right) \cong 18K\Omega$$

The overall transfer function of the TL431 and the optocoupler can be expressed as follows :

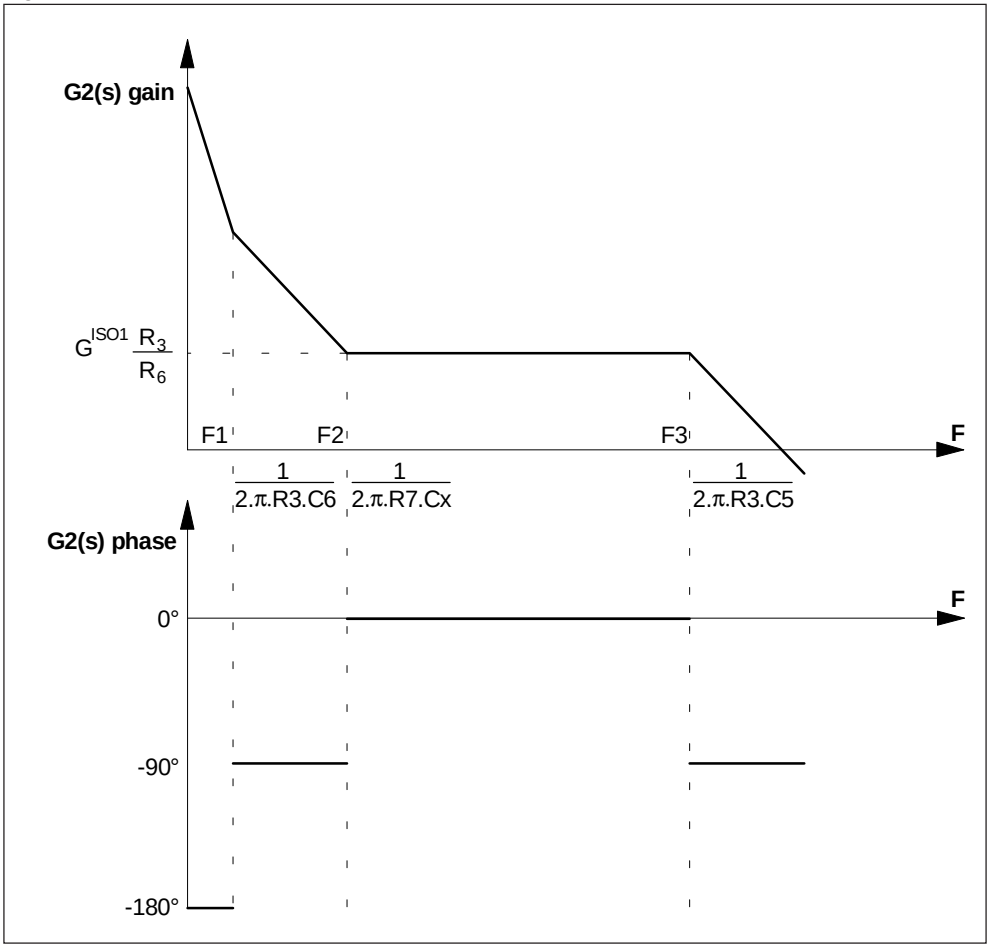
$$G2(s) = \frac{V_{COMP}}{V_{out}} = \frac{V_{COMP}}{Id} \bullet \frac{Id}{V_{out}} = -G^{ISO1} \bullet \frac{1 + R_3 \bullet C_6 \bullet s}{(C_5 + C_6) \bullet s \bullet \left(1 + R_3 \bullet \frac{C_5 \bullet C_6}{C_5 + C_6} \bullet s\right)} \bullet \frac{1}{R_6} \bullet \frac{1 + R_7 \bullet C_X \bullet s}{R_7 \bullet C_X \bullet s}$$

Taking into account that C5 is much smaller than C6 :

$$G2(s) = -G^{ISO1} \bullet \frac{1 + R^3 \bullet C^6 \bullet s}{C_6 \bullet s \bullet (1 + R_3 \bullet C_6 \bullet s)} \bullet \frac{1}{R_6} \bullet \frac{1 + R_7 \bullet C_X \bullet s}{R_7 \bullet C_X \bullet s}$$

This transfer function can be represented by the following theoretical phase and gain diagram (The formula for the negative sign has been omitted) :

**Figure 23.** Theoretical Gain and Phase behaviour



As it can be seen, a flat gain with a zero phase value extends from F2 to F3. The bandwidth of the regulation loop must lie in this range. First set of components value :

*1)To fix F3 at the zero of the power cell. This gives C5.*

*2)To cross 0 dB for the overall transfer function at 1/3 of the frequency where is located the zero of the power cell. This crossing frequency is named Fco. This gives R6.*

*3)To fix F2 at 1/10 of Fco. This gives Cx.*
Therefore, for the condition 2), we have:

$$FCO = \frac{2450}{3} = 817Hz$$

$$G2(s)_{817Hz} = [(\log 817 - \log 30) \bullet 20 - 12] =$$

$$= 16.73dB$$

At this point we can calculate C5, R6 and Cx:

$$C5 = \frac{1}{2 \bullet \Pi \bullet R_3 \bullet F3} = \frac{1}{6.28 \bullet 1 \bullet 10^3 \bullet 2450} \cong$$

$$\cong 68nF \text{ and,}$$

$$Cx = \frac{1}{2 \bullet \Pi \bullet R_7 \bullet (F_{CO}/10)} =$$

$$= \frac{1}{6.28 \bullet 18 \bullet 10^3 \bullet 80} \cong 100nF$$

And, considering an optotransistor with $G^{ISO1} = 0.5$,

$$R6 = \frac{G^{ISO} \bullet R_3}{G2(s)_{FCO}} = \frac{0.5 \bullet 1 \bullet 10^3}{6.86} \cong 82\Omega$$

At this point, considering $V_{FB}^{ISO1} = 1V$, we can calculate R8 as,

$$R_8 = \frac{V_{FB}^{ISO1} + R6 \bullet \frac{I_{COMPHI}}{G^{ISO1}}}{I_B^{U2}} =$$

$$= \frac{1 + 82 \bullet \frac{600 \bullet 10^{-6}}{0.5}}{1 \bullet 10^{-3}} \cong 1.2K\ \Omega$$

The last step is to calculate the zero due to R3 and C6, as:

$$F1 = \frac{1}{2 \bullet \Pi \bullet R_3 \bullet C_6} = \frac{1}{6.28 \bullet 1 \bullet 10^3 \bullet 1 \bullet 10^{-6}} =$$

$$= 159Hz$$

The same procedure can be repeated at min load (for this example 5W that leads to a $R'_0 = 28.8\Omega$

The gain Bode diagrams at max load and min load are represented in figures 24 and 25, while the phase Bode diagram for both cases is represented in figure 26.

**Figure 24.** Gain Bode Plot at Max Load

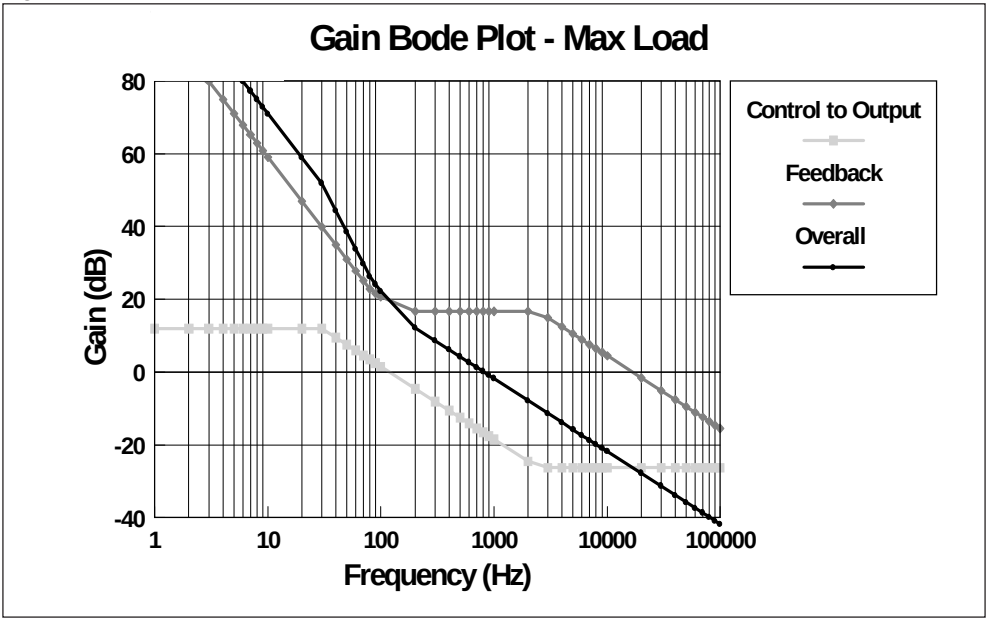


**Figure 25.** Gain Bode Plot at Min Load

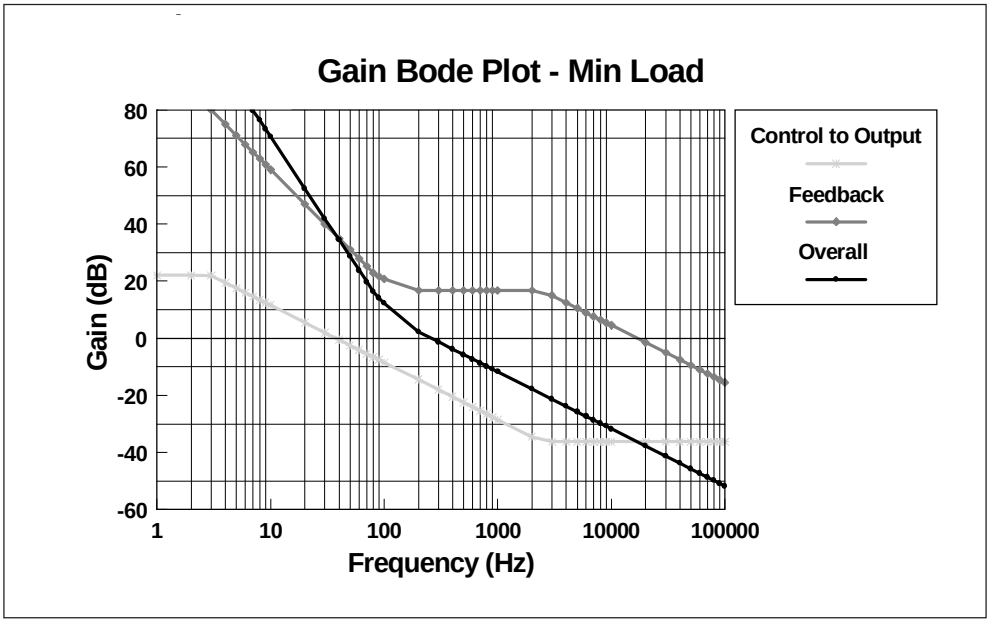
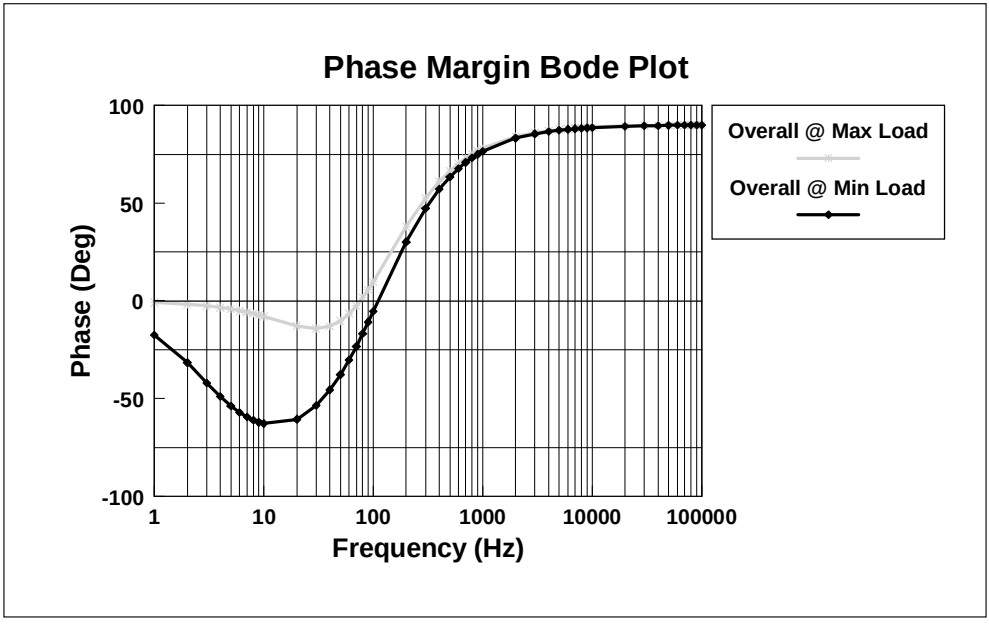



**Figure 26.** Phase Margin Bode Plot



# *Appendix A:*

## OUTPUT LOAD DOUBLING IN DISCONTINUOUS FLYBACK

### Scope

This document gives some explanation on the fact that the effective power cell pole of a discontinuous flyback is the double of the one of the load itself, when this load is constituted of a filtering capacitor and the load resistor. It can be also extended very easily to other types of loads, like constant current or constant voltage absorber (Batteries).

### Pole doubling explanation

A discontinuous flyback can be considered as a constant power source. Each cycle delivers always the same energy, whatever the output voltage. This elementary energy can be conventionally expressed as :

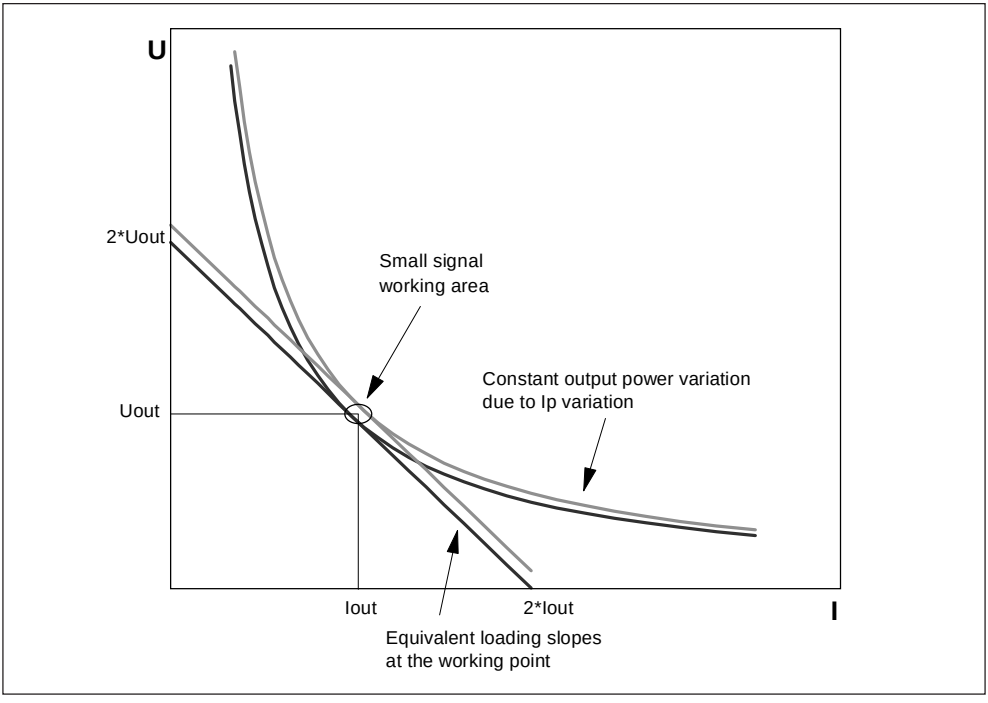
$$E_{OUT} = ½ \bullet L_P \bullet I_P^2$$

A modulation of the input (Compensation voltage) of the power cell makes some small changes on the Ip value, thus modifying the level of energy sent on secondary side. Therefore, in figure 27 the following curves can be established, showing the U-I characteristics of the converter output.

The tangential slopes to the constant power curves at the working point give the equivalent characteristic of the power cell. The constant power curves being hyperbolas, it can be demonstrated that the intersection of these slopes with the X and Y axis are respectively 2*Iout and 2*Uout. Therefore, the power cell can be identified with a voltage generator of which the value is 2*Uout, and the output impedance Zout is :

$$Zout = \frac{2 \bullet U_{out}}{2 \bullet I_{out}} = R_L$$

**Figure 27.** U-I characteristics of the converter output :

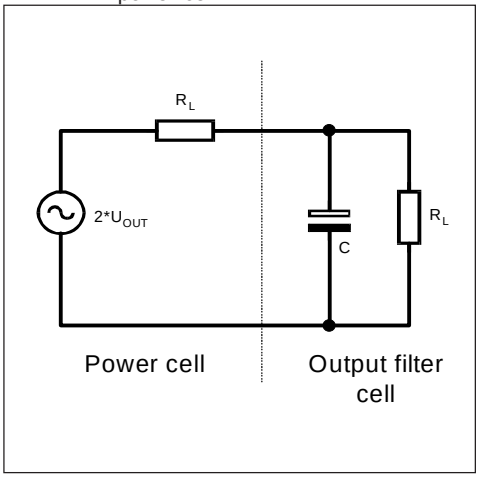


Where $R_L$ is the output load. The total equivalent schematics of the converter power cell can be represented in the following manner in figure 28. And the output power cell pole $F_P$ can be computed as :

$$F_P = \frac{1}{2 \cdot \Pi \cdot \frac{R_L}{2} \cdot C} = \frac{1}{\Pi \cdot R_L \cdot C}$$

It appears that this pole has a value twice higher than the conventional one computed directly from the simple observation of the output filter. The ESR of the capacitor C can also be added.

**Figure 28.** equivalent schematics of the converter power cell




The output load $R_L$ can be replaced by a constant current source or a constant voltage to obtain the corresponding transfer functions of the total power cell. Note that in the case of a constant current source, we find a pole at:

$$p = \frac{1}{2 \cdot \Pi \cdot R_L \cdot C}$$

which is not so easy to guess from the normal schematics, and which really exists!

## Measurement

A transferometer has been used to verify the above results. This apparatus has a sinusoidal generator and two analyser channels. It is able to give directly the transfer function of a circuit by doing the phase and gain ratio between the two channels. The schematics have been used with the standard 12V VIPer100 demoboard.

The generator is connected on the VDD supply, after the filtering capacitor. By doing so, the normal working point of the converter is not changed. The first analyser channel is connected on the compensation pin, and the second one on the output. The transfer function of the power cell is CH2/CH1. The results can be seen in figure 30.

The pole is a little bit more than 20Hz, and the zero at 550Hz. This can be observed from the phase crossing the -45° axis, or from gain variation of 3 dB. Here are the computations from standard formulas :

$$\frac{1}{2 \cdot \Pi \cdot R_5 \cdot C_6} = 10.6\text{Hz} \quad \text{and}$$

$$\frac{1}{2 \cdot \Pi \cdot R_4 \cdot C_6} = 557\text{Hz}$$

**Figure 29.** Measurement Schematic

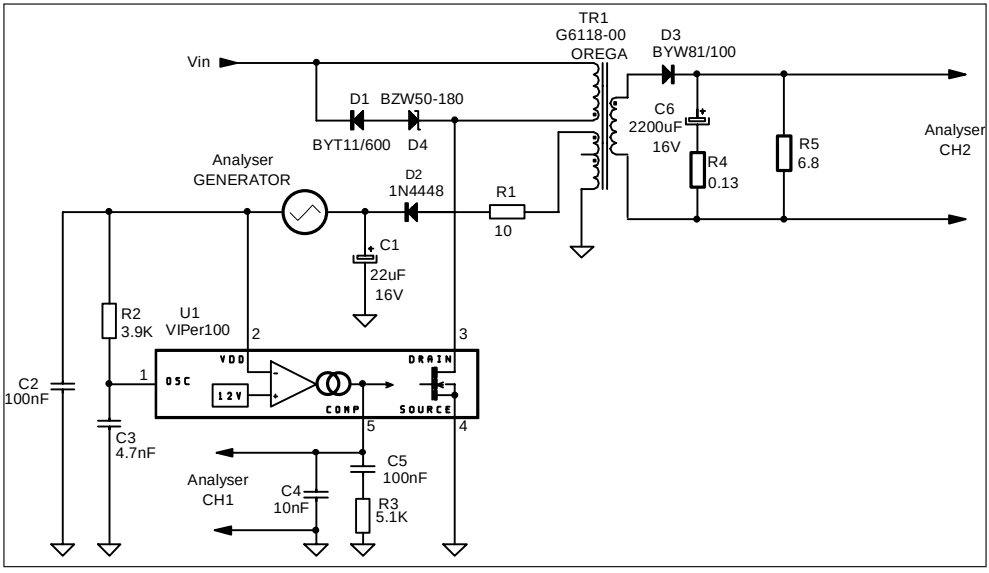



**Figure 30.** Transfer function of the power cell